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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,426	06/29/2001	Sunetra K. Mendis	VISA-56	2277

28112 7590 06/15/2005

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EXAMINER	
VIEAUX, GARY	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,426	MENDIS ET AL.	
	Examiner	Art Unit	
	Gary C. Vieaux	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 20* is/are rejected.

7)☒ Claim(s) *18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

The Amendment filed on February 10, 2005 has been received and made of record. In response to the first office action, the Specification, the Drawings, and claims 1, 2, 9, and 10 have been amended.

Response to Amendments

In response to Applicant's amended Drawings, the Examiner finds the amended figure 1 to be properly designated as Prior Art, and therefore, this objection to the Drawings is hereby withdrawn.

In response to Applicant's amended Specification, the Examiner finds the amendments to correct the Specification, in relation to providing proper antecedent basis for the claimed subject matter, without adding new matter, and therefore the objections to the Specification and the 35 USC §112 rejection to claims 18 and 19 are hereby withdrawn.

Response to Arguments

Applicant's arguments with respect to figure 1, as they to a Bayer pattern color mosaic, have been fully considered and are persuasive. Therefore, the objection to figure 1 of the Drawings is hereby withdrawn.

Applicant's arguments with respect to claims 2, and 10, see Remarks p. 9, have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claim 9, see Remarks p. 9, have been fully considered but they are not persuasive. Applicant contends that claim 9 can be differentiated from Rambaldi in that the bad pixels of claim 9 correspond to bad unit cells, whereas in Rambaldi, bad pixels correspond to bad color cells. The Examiner respectfully disagrees. Claim 9, as currently written, does not contain limitations relating to "unit cells", and therefore further discussion is considered moot. Additionally, the color pixel array illustrated in fig. 5 and discussed in column 11 lines 15-31 of Rambaldi, although not explicitly named, is of the configuration commonly known as the "Bayer Pattern" and therefore is accepted as such without explicit reference. Based on the foregoing, the Examiner stands behind the rejection.

Applicant's arguments with respect to claim 17, see Remarks p. 9, have been fully considered but they are not persuasive. Applicant contends that the Examiner's reading of the claim is no longer valid. The Examiner respectfully disagrees. Claim 17, as it is currently written, does not distinctly preclude a reading in which disconnection and connection are equated with memory entries. Therefore, the Examiner stands behind the rejection.

The Examiner notes that the Applicant made no remarks at this time regarding claim rejection on the merits of claims 1, 3-8, 11-16 or 18-20.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-4 and 6-9, 11-12, 14-17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rambaldi et al. (US 6,618,084.)

Regarding claim 1, Rambaldi teaches a method for improving a CMOS active image sensor chip that includes an array of pixels, comprising: providing, on said chip, a directory for storing pixel addresses (col. 3 lines 49-52); testing the pixel array to determine at which addresses bad pixels are located (fig. 4A); permanently storing in said directory said bad pixel addresses (fig. 4A step 516; col. 3 lines 36-39; col. 5 lines 47-48); checking the directory to determine if any given pixel of the sensor array is bad (fig. 4B step 536); if a particular pixel is found to be bad, thereby showing that its signal is spurious, transferring signal intensity data from the bad pixel's nearest neighbors into a buffer memory (fig. 4B steps 538, 554; col. 10 lines 21-37); from said nearest neighbor data, computing a replacement value for the bad pixel (fig. 4B step 552; col. 10 lines 10-15); and substituting said replacement value for said bad pixel signal value (fig. 4B step 554.)

Regarding claim 3, Rambaldi teaches all the limitations of claim 3 (see the 102(e) rejection to claim 1 supra), including teaching a method wherein the step of computing replacement signal data from nearest neighbors and then transferring it to the array is performed on the chip (fig. 1 indicator 10; col. 5 lines 30-34.)

Regarding claim 4, Rambaldi teaches all the limitations of claim 4 (see the 102(e) rejection to claim 1 supra), including teaching a method wherein the step of computing replacement signal data from nearest neighbors and then transferring it to the array is performed on a separate chip (col. 5 lines 30-34.)

Regarding claim 6, Rambaldi teaches all the limitations of claim 6 (see the 102(e) rejection to claim 1 supra), including teaching a method wherein said nearest neighbors are in the same row as the bad pixel (col. 2 lines 46-57; col. 11 lines 24-28.)

Regarding claim 7, Rambaldi teaches all the limitations of claim 7 (see the 102(e) rejection to claim 1 supra), including teaching a method wherein said nearest neighbors are in the same column as the bad pixel (col. 2 lines 46-57.)

Regarding claim 8, Rambaldi teaches all the limitations of claim 8 (see the 102(e) rejection to claim 1 supra), including teaching a method wherein said nearest neighbors are in the same diagonal as the bad pixel (col. 2 lines 46-57; col. 11 lines 24-28.)

Regarding claim 9, Rambaldi teaches a method for improving a Bayer pattern color mosaic (fig. 5), comprising: providing said Bayer pattern color mosaic in the form of a chip having an array of alternating blue-green and red-green sensors (fig. 5); providing, on said chip, a directory for storing pixel addresses (col. 3 lines 49-52); testing the pixel array to determine at which addresses bad pixels are located (fig. 4A);

permanently storing in said directory said bad pixel addresses (fig. 4A step 516; col. 3 lines 36-39; col. 5 lines 47-48); checking the directory to determine if any given pixel of the sensor array is bad (fig. 4B step 536); if a particular pixel is found to be bad, thereby showing that its signal is spurious, transferring signal intensity data from the bad pixel's nearest neighbors of the same color into a buffer memory (fig. 4B steps 538, 554; col. 11 lines 16-28); from said same-color nearest neighbor data, computing a replacement value for the bad pixel (fig. 4B step 552; col. 11 lines 24-28); and substituting said replacement value for said bad pixel signal value (fig. 4B step 554.)

Regarding claim 11, Rambaldi teaches all the limitations of claim 11 (see the 102(e) rejection to claim 9 supra), including teaching a method wherein the step of computing replacement signal data from same-color nearest neighbors and then transferring it to the array is performed on the chip (fig. 1 indicator 10; col. 5 lines 30-34.)

Regarding claim 12, Rambaldi teaches all the limitations of claim 12 (see the 102(e) rejection to claim 9 supra), including teaching a method wherein the step of computing replacement signal data from same-color nearest neighbors and then transferring it to the array is performed on a separate chip (col. 5 lines 30-34.)

Regarding claim 14, Rambaldi teaches all the limitations of claim 14 (see the 102(e) rejection to claim 9 supra), including teaching a method wherein said same-color nearest neighbors are in the same row as the bad pixel (fig. 5; col. 2 lines 46-57; col. 11 lines 24-28.)

Regarding claim 15, Rambaldi teaches all the limitations of claim 15 (see the 102(e) rejection to claim 9 supra), including teaching a method wherein said same-color nearest neighbors are in the same column as the bad pixel (fig. 5; col. 2 lines 46-57.)

Regarding claim 16, Rambaldi teaches all the limitations of claim 16 (see the 102(e) rejection to claim 9 supra), including teaching a method wherein said same-color nearest neighbors are in the same diagonal as the bad pixel (fig. 5; col. 2 lines 46-57; col. 11 lines 24-28.)

Regarding claim 17, Rambaldi teaches a method for improving a pixel array, comprising: testing the pixel array to determine at which address a bad pixel is located (fig. 4A); disconnecting said bad pixel from the array (fig. 4A step 516; in which "disconnecting" is equated with the storing of the bad pixel address in memory); and connecting one or more of said bad pixel's nearest neighbors to the array at said address, whereby said nearest neighbors serve, in combination, as a replacement for said bad pixel (fig. 4B step 554; col. 10 lines 10-15; in which "connecting" is equated with the association of nearest neighbor data.)

Regarding claim 20, Rambaldi teaches all the limitations of claim 17 (see the 102(e) rejection to claim 17 supra), including teaching a method wherein said nearest neighbors are in the same row as the bad pixel (col. 2 lines 46-57; col. 11 lines 24-28.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rambaldi et al. (US 6,618,084), in view of Hamdy et al. (US 4,899,205.)

Regarding claim 2, Rambaldi teaches all of the elements of claim 2 (see the 102(e) rejection to claim 1 supra) except for teaching wherein the step of permanently storing the bad addresses further comprises using fusible link technology or anti-fuse technology.

Nevertheless, Nova provides a teaching of anti-fuse technology applied to memory (col. 12 lines 36-53.) It would have been obvious to one of ordinary skill in the art at the time of the invention to employ anti-fuse technology with the method as taught by Rambaldi, in order to create non-volitile storage of the bad pixel addresses.

Regarding claim 10, Rambaldi teaches all the limitations of claim 10 (see the 102(e) rejection to claim 9 supra), except for teaching a method wherein the step of permanently storing the bad addresses further comprises using fusible link technology or anti-fuse technology.

Nevertheless, Nova provides a teaching of anti-fuse technology applied to memory (col. 12 lines 36-53.) It would have been obvious to one of ordinary skill in the

art at the time of the invention to employ anti-fuse technology with the method as taught by Rambaldi, in order to create non-volitile storage of the bad pixel addresses.

Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rambaldi et al. (US #6,618,084), in view of Examiner's Official Notice.

Regarding claim 5, Rambaldi teaches all the limitations of claim 5 (see the 102(e) rejection to claim 1 supra), except for directly teaching a method wherein the step of computing replacement signal data from nearest neighbors and then transferring it to the array is performed on a host computer. Official Notice is taken regarding pixel correction being performed by software found on a host computer; a concept that is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a host computer to compute replacement signal data from nearest neighbors and then transfer it to the array in order to conserve chip real estate.

Regarding claim 13, Rambaldi teaches all the limitations of claim 13 (see the 102(e) rejection to claim 9 supra), except for directly teaching a method wherein the step of computing replacement signal data from same-color nearest neighbors and then transferring it to the array is performed on a host computer. Official Notice is taken regarding pixel correction being performed by software found on a host computer; a concept that is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a host computer

to compute replacement signal data from same-color nearest neighbors and then transfer it to the array in order to conserve chip real estate.

Allowable Subject Matter

Claims 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 18, the prior art is not found to teach or fairly suggest, in combination with the claims from which dependence is derived, wherein the steps of disconnecting said bad pixel from, and connecting one or more nearest neighbor pixels to, the array further comprises using fusible link technology or anti-fuse technology.

Regarding claim 19, the prior art is not found to teach or fairly suggest, in combination with the claims from which dependence is derived, wherein the step of testing the pixel array to determine at which address a bad pixel is located is performed prior to dicing into chips, thereby enabling the steps of disconnecting said bad pixel from, and connecting one or more nearest neighbor pixels to, the array to be accomplished by means of chip-level wiring.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Foster (US 2002/0145507 A1) discloses the use of anti-fuse technology where one-time programming of non-volatile memory is required.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary C. Vieaux whose telephone number is 571-272-7318. The examiner can normally be reached on Monday - Friday, 8:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary C. Vieaux
Examiner
Art Unit 2612

Gcv2

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PRIMARY EXAMINER